Source/Drain Adjust Implant

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A two-transistor PMOS memory cell includes a PMOS floating gate transistor sharing a drain/source P+ diffusion region with a PMOS select gate transistor. The shared drain/source diffusion region acts as a drain for the floating gate transistor and as a source to the select gate transistor. The shared drain/source P+ diffusion region is formed in an N- well. Underlying the drain/source P+ diffusion region is a N implant having the same lateral extent of the drain/source P+ diffusion region to provide a lower programming voltage for the floating gate transistor and improved punch-through resistance for the select gate transistor.